AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph 0024 of the specification with the following paragraph having revision marking to show changes made:

The gate terminals of the fifth NMOSFET N105 and the eighth PMOSFET P108 are configured to receive the first part (VIN-) of a differential input signal, while the gate terminals of the sixth NMOSFET N106 and the seventh PMOSFET P107 are configured to receive the second part (VIN+) of the differential input signal. To increase the gain of the operational amplifier 111, cascoded MOSFETS may be disposed between the sixth PMOSFET P106 and the output terminal 111 and between the fourth NMOSFET N104 and the output terminal 111. For example, cascoded PMOSFET P110 may optionally be disposed between PMOSFET P106 and output terminal 111. Furthermore, cascoded NMOSFET N108 may optionally be disposed between NMOSFET N104 and the output terminal 111.

Please replace the paragraph 0038 of the specification with the following paragraph having revision marking to show changes made:

Figure 3 illustrates an alternative comparator 300 with an alternative operational amplifier 310 and inverter 320. The comparator 300 of Figure 3 is similar to the comparator 100 of Figure 1, except that PMOSFETs P101 through P109 are replaced by NMOSFETs N301 through N309, respectively, with their source terminals coupled to the lower voltage level rather than the higher voltage level. Also, the NMOSFETs N101 through N107 are replaced by

PMOSFETs P301 through P307, respectively, with their source terminals coupled to the higher voltage level rather than the low voltage level. Also, the source terminals of the fifth and sixth PMOSFETs P305 and P306 are coupled to a current source I301, while the source terminals of the seventh and eighth PMOSFETs N307 and N308 are coupled to a current sink I302. Furthermore, cascoded NMOSFET N108 is replaced by cascoded PMOSFET P308, while cascoded PMOSFET P110 is replaced by cascoded NMOSFET N310.